**PROGRAMMABLE I/O INTERFACES FOR FPGAs AND OTHER PLDs**


ABSTRACT

A programmable logic device (PLD), such as a field programmable gate array (FPGA) has a logic core surrounded on one or more sides by an input/output (I/O) interface having one or more programmable I/O buffers (PIBs). At least one PIB can be programmed to perform two or more of (a) a pass-through data input mode, (b) an input register mode; (c) a double data rate (DDR) input mode, (d) one or more demux input modes, (e) one or more DDR demux input modes. In addition or alternatively, at least one PIB can be programmed to perform two or more of (a) a pass-through data output mode, (b) an output register mode, (c) a DDR output mode, (d) one or more mux output modes, and (e) one or more DDR mux output modes. As such, devices of the present invention are flexible enough to support both low-rate and high-rate interface applications, while efficiently using device resources.